IN THE SPECIFICATION

The specification was objected to regarding an update of a serial number to reflect an issued patent number. The specification was further objected to, requesting that "Figures 12A-12N be rewritten to describe each claim individually." Please amend the specification as follows:

The paragraph beginning on page 1, under the title is amended as follows:

This application is a Continuation of U.S. Serial No. 08/842030 filed on April 23, 1997, now issued as U.S. Patent No. 6,175,891.

The paragraph beginning on page 8, line 14 is amended as follows:

~~Figures 12A - 12N are diagrams representing exemplary interface registers used in carrying out various memory operations.~~

Figure 12A is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12B is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12C is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12D is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12E is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12F is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12G is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12H is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12I is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12J is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12K is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12L is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12M is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Figure 12N is a diagram representing a number of interface registers used in carrying out various memory operations according to an embodiment of the invention.

Reconsideration and withdrawal of the objections to the specification is respectfully requested.